a first control circuit, connected between the delay circuit and the second drive circuit, for receiving the input signal and the delayed output signal and generating first control signal for driving the second drive circuit after the output signal is changed by a predetermined amount.

A marked-up copy of the amended claims is attached as required under 37 CFR §1.121.

REMARKS

The above amendments and the following remarks are fully and completely responsive to the Office Action dated December 11, 2001. Claims 1-11 are pending in this application. No new matter has been entered. Claims 1-11 are presented for reconsideration.

In the outstanding Office Action, claims 1-11 were rejected under 35 USC §102(b) as being anticipated by Wert (U.S. Patent No. 6,281,706). In making this rejection, the Office Action asserts that Wert teaches each and every element of the claimed invention. Applicants request reconsideration and withdrawal of this rejection.

Claim 1 recites a method of controlling an output buffer circuit that includes a first drive circuit for receiving an input signal having a sharp waveform and for generating an output signal that has a gentle wave form and is output from an output terminal of the output buffer circuit. A second drive circuit is connected to the output terminal and has a lower output impedance than the first drive circuit. The method includes changing the output signal in accordance with the change in the input signal using the first drive circuit. The second drive circuit is driven after the output signal is changed by a predetermined amount.

Accordingly, the present invention, as set forth in claims 1 and 2, is directed to a method for controlling an output buffer circuit including a first drive circuit and a second drive circuit. The method includes driving the second drive circuit after an output signal of the buffer circuit (the first drive circuit) is changed by a predetermined amount.

The present invention, as set forth in claim 5, is also directed to an output buffer that includes a first drive circuit, a second drive circuit, a delay circuit, and a control circuit. The control circuit generates a control signal for driving the second drive circuit after an output signal of the buffer circuit is changed by a predetermined amount. Consequently, after the signal output by the first drive circuit changes by the predetermined amount, the second drive circuit having a low output impedance characteristic is driven so that the low output impedance characteristic is provided in the static state of the output signal.

Wert is directed to a programmable high speed quiet I/O cell that uses a first drive circuit (701, 711) and a boost or second drive circuit (705, 717). When transitioning from a logic low to a logic high, Wert teaches that because of propagation delay, transistor 705 is turned on after transistor 701. Because of the relative threshold voltages, transistor 705 is turned off before transistor 701. Wert also teaches that during a logic high to a logic low transition, transistor 717 is turned on after transistor 711 and then turned off before transistor 711 is turned off. Consequently, the second drive circuit (705, 717) of Wert is only driven while the first drive circuit (701, 711) is driven.

In contrast, the present invention, as set forth in claims 1, 2 and 5, recites driving the second drive after the output signal is changed by a predetermined amount. Wert does not and cannot teach driving the second drive circuit after the output signal of the first drive circuit changes because the second drive circuit is only driven while the first drive circuit is driven. Accordingly, the present invention is neither disclosed nor suggested by Wert. Furthermore, due to the differences between the present invention and Wert, Wert is unable to provide the advantages of the present invention. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-2 and 5 under 35 USC §102(b).

Claims 3-4 and 6-11 depend either directly or indirectly from claims 2 and 5 respectively. Therefore, it is respectfully submitted that these claims are not anticipated by or obvious in view of Wert for at least the reasons set forth with regard to claims 1, 2 and 5 above.

Applicants amendments and remarks clearly overcome the rejections set forth in the Office Action dated December 11, 2001. Specifically, applicants remarks have distinguished claims 1-11 from Wert, and thus have overcome the rejection of these claims under 35 USC §102(b). Consequently, claims 1-11 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 1-11.

Applicants submit that the application is now in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned Attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300 making reference to Attorney Docket No. 108075-00022.

Respectfully submitted,

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MARKED-UP COPY OF AMENDED CLAIMS
AS REQUIRED UNDER 37 CFR §1.121

2. (Amended) A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor connected between a first power supply and an output terminal of the output buffer circuit and a second output transistor connected between a second power supply and the output terminal, wherein the first and second output transistors generate an output signal having gentle waveform in response to an input signal having a sharp waveform, the second drive circuit including a third output transistor connected between the first power supply and the output terminal and a forth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors, the method comprising the steps of:

generating the output signal in accordance with the input signal using the first drive circuit;

generating a delay signal by delaying the output signal;

generating a control signal for controlling the third and fourth output transistors in accordance with the delay signal and the input signal; and

driving the second drive circuit in accordance with the control signal <u>after the output signal is changed by a predetermined amount.</u>

5. (Amended) An output buffer circuit comprising:

a first drive circuit for receiving an input signal having a sharp waveform and generating an output signal that has a gentle waveform and is output from an output terminal of the output buffer circuit;

a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit;

a delay circuit, connected to the output terminal, for delaying the output signal and generating a delayed output signal; and

a first control circuit, connected between the delay circuit and the second drive circuit, for receiving the input signal and the delayed output signal and generating first control signal for driving the second drive circuit <u>after the output signal is changed by a predetermined amount.</u>